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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,841	10/08/2004	G. R. Mohan Rao	A4-1845	5840

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
01/31/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/711,841	RAO ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7-21,23-28 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27,28 and 30* is/are allowed.

6)☒ Claim(s) *1,4,5,7-12,15-21,23 and 25* is/are rejected.

7)☒ Claim(s) *3,13-14,24,26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 11/26/2007 has been entered.

2. Claims 1, 3-5, 7-21,23-28, 30 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 3-5, 7-2, 23-28,30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 9-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Roohparvar (Pub. U,S, Patent No. 2004/0039870).

Regarding claims 9-10, Roohoarvar discloses a semiconductor memory device (Figure 2) comprising a bank with multiple pages, the device comprising means (Figure 1, 170, [0024] ACTIVE command) for keeping multiple pages open on the bank ([0025], open page having length of 8000bits), wherein the keeping means comprises latches (Figure 1, 150, [0022], Read/Latch, Figure 2, 210) coupled to a sense amplifier ([0025], sense amplifiers circuit) associated with the bank ([0024]), the latches (Figure 2, 1000 latches. [0025]) operating in the storage of data read-from and written-to the sense amplifier, wherein the device is a nonvolatile memory device (ABSTRACT) with multiple pages open in a block (Figure 2, 220) or sector thereof, and wherein the device is a flash memory device ([0002]).

6. Claims 1, 4-5, 7-9, 21, 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki (Pub. U.S. Patent No. 2004/0165472).

Regarding claims 9, 19, Yamazaki discloses a semiconductor memory device (Figure 2) comprising a bank with multiple pages (Figure 2, 10) , the device comprising means (page mode) (Figure 3, REPM, KEEP PAGE OPEN) for keeping multiple pages open ([0087], opened page maintained open) on the bank, wherein the keeping means comprises latches coupled to a sense amplifier ([0345], [0349]) associated with the bank, the latches operating in the storage of data read-from and written-to the sense amplifier (Figure 5, SA, [0347]), wherein the device is a nonvolatile memory device ([0384]) with multiple pages open in a block or sector thereof.

Regarding claims 1, 11, 16, 21, Yamazaki discloses a semiconductor memory device and a method comprising keeping open more than one page of multiple pages on a bank of a semiconductor memory device and posting a precharge command ([0088]) immediately after a command ([0088], read operation) for a first access of one of the multiple pages in anticipation of a subsequent access of the page ([0089]), wherein the keeping step is performed with latches coupled to a sense amplifier associated with the bank, the latches operating in the storage of data read-from and written-to the sense amplifier (Figure 5, SA).

Regarding claims 4, 12, Yamazaki discloses wherein the bank comprises memory cells arranged in arrays of rows and columns (Figure 5), and the keeping means comprises a counter ([0017]) in a row path operatively connected to the rows of the bank.

Regarding claims 5, 15, Yamazaki discloses wherein the device comprises a SRAM ([0023]) register coupled to the sense amplifier to provide low column access latency ([0249], column latency).

Regarding claims 7, 17, Yamazaki discloses wherein bank comprises memory cells arranged in arrays of rows and columns, the memory cells comprise storage cells, and the storage cells comprise at least one transistor and at least one capacitor ([0002-0003].

Regarding claims 8, 18, Yamazaki discloses wherein the device has a dynamic random access memory architecture ([0002]).

Regarding claim 23, Yamazaki discloses wherein the page is kept open for a number of clock cycles following the precharge command and the precharge command causes a precharge operation to be executed ([0087-0088]) after completion of the number of clock cycles ([0086], one clock cycle).

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Lu (U.S. Patent No. 6,023,745).

Regarding claims 9-10, Lu discloses a semiconductor memory device (Figure 1) comprising a bank (ABSTRACT) with multiple pages (ABSTRACT), the device comprising means for keeping multiple pages open on the bank (STRACT), wherein the keeping means comprises latches coupled to a sense amplifier associated with the bank (Figure 4, Column 7, lines 41-62), the latches operating in the storage of data read-from and written-to the sense amplifier (Figure 8, 801), wherein the device is a nonvolatile memory device (Column 24, lines 1-20) with multiple pages open in a block or sector thereof, and wherein the device is a flash memory device (Colum 2, lines 1-3).

8. Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Taylor et al. (U.S. Patent No. 5,835,965).

Regarding claim 9, Taylor et al. disclose a semiconductor memory device (Figure 7) comprising a bank (600) with multiple pages (Column 1, lines 58-65), the device comprising means for keeping multiple pages open on the bank (column 8, lines 45-47), wherein the keeping means comprises latches (Column 45-47) coupled to a sense amplifier (Column 8, lines 57-62) associated with the bank, the latches operating in the storage of data read-from and written-to the sense amplifier, wherein the device is a nonvolatile memory device (column 18, lines 3-5) with multiple pages open in a block or sector (Column 9, lines 60-61) thereof.

Allowable Subject Matter

9. Claims 3, 13-14, 24,26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3, 13-14, 24 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. The prior art does not teach the claimed invention having a means for resetting the keeping means if the subsequent access of the page occurs while the page is open, the resetting means operating to further delay execution of the precharge operation initiated by the precharge command.

10. Claims 27-28, 30 are allowed.

Claims 27-28, 30 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest

the claimed limitations. The prior art does not teach the claimed invention having a method comprising keeping open more than one page of multiple pages on a bank of a semiconductor memory device, wherein the keeping step is performed with latches coupled to • a sense amplifier associated with the bank, the latches operating in the storage of data read-from and written-to the sense amplifier, the bank comprises memory cells arranged in arrays of rows and columns, and a precharge command is performed by a precharge counter that, when a row address is latched and a page is opened, the counter locks into the row address until reset, and when the precharge command is made, an internal activation for performing a precharge operation is activated after a predetermined number of clock cycle.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827